

# EUVL HVM Insertion Timing and Scaling

**Panel Discussion**  
**2012 International Workshop on EUV Lithography**  
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# Topic 1

## Timing of EUV HVM Insertion for the Industry?

### Minimum Throughput Needs?

#### By Device

- NAND
- DRAM
- IDM
- Foundry

#### By Function

- Line/Space
- CON/Via

# Topic 2

## EUV Ecosystem Requirements?

- Changes relative to 193nm infrastructure and critical issues to resolve.

## Minimum Requirements?

- Source Power
- OPC needs
- Mask Requirements (Defects, cleans and Metrology)
- Resist Issues

# Topic 3

## EUVL scaling paths to meet the ITRS timelines for 5-7nm nodes (2017-2020)?

- Lower K1/Double Patterning
- NA scaling to  $NA > 0.5$
- 6.8nm Soft X-ray Lithography  
New infrastructure (optics, resists, power requirements again)

# Panel Input

**Yan Borodovsky**

- 1. EUV will compete with 193i. Will need >100WPH and Yield/COO for HVM.**
- 2. Logic Complementary and DRAM CON will be first.**
- 3. EUV Source Power Target Will Need to be Re-targeted (1000W) at IF for Stochastic Suppression (Driven by Shot Noise Statistics). OPC is complex. New Ideas Critical.**
- 4. 2015-2017:- >1.7kW @ IF, stay at 13.5nm, Advanced Illumination, DPT.**

# Takashi-Kamo San

## **1. DUV Inspection + EB Repair.**

**EUV-AIMS not available for early stage of HVM**

**→ 3D-SEM and Lithography Simulation Utilized As Alternative.**

**Challenging to predict defect printability without EUV-AIMS.**

## **2. Actinic Blank Inspection Under Development for 1x HP (EIDEC) Defect Mitigation Strategies Under Development.**

## **3. Mask Materials Will Need Optimization for higher NA New Materials for Lower Wavelength. (further R&D needed).**

## **4. Mask CD's/Absorber Patterns can scale to 1xnm hp single exposure. (4xnm on mask)**

# Pawitter Mangat

1. **Fab COO, Integration Demos, CD/OL Budgets.**  
**193i benchmarking is key.**  
**Earliest HVM timeline ~ 2016, Source Power 1<sup>st</sup> ....**  
**OPC intensity needs attention/work.**
2. **CON/Via Levels First Layers of Choice ...**
3. **Blank Fiducials Add:- Defect Delta Needs Characterizations.**  
**Killer Defects:- How do we Identify?**  
**Focus on defect printability.**
5. **EUV DPT an Option, Sensitive to Costs.**  
**MAKE 13.5nm EUVL Work ....**

# BackUp